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Robust Optimization of a Lead Free SMT Process

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Abstract
This paper will focus on Dr. Taguchi's Robust Engineering methodology, measurement methods and experimental results for the optimization of a lead free SMT process for use in an Automotive Electronics application. The key strategy is to find process parameters that make the process insensitive to noise factors. Traditional optimization approaches focus on maximizing the response variable while the Robust approach focuses on consistent results regardless of variation in noise factors.

The Robust method was utilized in the development of a lead free process for manufacturing an Automotive SMT product. Major factors that can create variation in a lead free process were identified, including lead free solder paste brand, paste print speed, oven reflow temperatures and times, and reflow environment. Several noise factors were studied including volume of solder paste, location of components on the board, and lead frame plating materials, namely tin and palladium/nickel/gold. A series of measurements were made on the lead free product that assessed the strength and reliability of lead free solder joints, measurements such as visual scoring, cross-section, surface insulation resistance, and pull strength. Using the Robust experimental design, these measurements were optimized to create high quality and reliable lead free SMT solder joints that were the most insensitive to the noise. In essence, quality was increased by using variable measurements rather than by counting attributes (good/bad). Overall, a gain of 2.1 dB was realized. In Robust terms, this equates to reducing variation in the lead free process by ~22%. This study also revealed which of the processing factors were most significant in controlling the lead free process. The results of this study and the use of Robust Engineering methodology provide a means for developing a full range of lead free technology, components and products used on Automotive Electronics.

Introduction
One of the challenging new fields in the electronics industry is the implementation of lead free into electronic products. This change is being driven primarily via legislation, especially in Europe, specifically through the WEEE and RoHS Directive in Europe, in its current revision banning the use of lead in electronics by 2006.[1, 2]

An essential element to developing these lead free products is the implementation of the lead free manufacturing process. The lead free manufacturing process poses new challenges not encountered in the traditional tin/lead world of electronics. One key difference in the lead free manufacturing footprint from traditional processes is the reduced wetting potential of the lead free solders that will be used. The physics of wetting dictate this reduced wetting since the lead free alloys have higher surface tensions than tin/lead systems, therefore making it more difficult to solder parts.[3]

In addition to the wetting challenges, lead free alloys require higher melting temperatures than their tin/lead counterparts, increasing the stresses on the components to be soldered. An important element to lead free manufacturing is limiting the maximum process temperatures and thermal energies to which components are exposed. For example, in the recently released IPC/JEDEC J-STD-020B, a component classification industry standard, lead free packaged parts are only required to be classified up to peak oven temperatures of 245°C or 250°C depending upon package size. Once a process is put into place that can produce soldered parts within such temperature requirements, only then can a sufficient component supply base be made available that can match product requirements.

For the automotive electronics industry, the reliability of the manufactured electronic product is important due to the stressful environments seen by these products. In this high volume business, first time quality (FTQ) must be high, and the need for an effectively optimized manufacturing process is an absolute requirement. This is especially true in the emerging field of lead free.

This paper discusses the optimization of a surface mount only (SMT) process for a lead free automotive electronics assembly process. SMT was chosen due to the drop-in replacement potential for this soldering technique, as opposed to wave soldering or selective soldering, which are much more immature fields in terms of lead free development.[4] This immaturity is partially the result of the huge capital investments that are necessary for wave soldering or selective soldering since dedicated soldering pots are required because Pb poisoning is problematic.[5] The Robust Engineering methodology was used to optimize this lead free SMT manufacturing process. This methodology is a powerful tool for selecting the best

manufacturing process parameters that mitigate manufacturing variation. This process will be discussed, as will the specifics of the lead free investigation.

Experimental

Robust Engineering Methodology

To evaluate the SMT lead free process for an automotive electronics assembly process, the Robust Engineering approach was used. In general, the Robust Engineering strategy is to find the combination of factors that produce the most consistent response, across various noise conditions. In other words, the goal is to achieve consistent response regardless of variations in manufacturing, environment, and customer's usage conditions.

The first step was to determine what response to measure. It was decided to optimize solder joint wetting and then verify strength of the optimum combination using thermal cycling. Pull strength was also evaluated; however, the repeatability of this response is suspect. Solder wetting was evaluated using visual scoring (numerical grading scale).

The second step was to identify the key process factors that effect wetting results. This was done by developing a Process Map for the SMT process (PMAP) and a Failure Mode & Effects Analysis table (FMEA). The PMAP is produced by "walking" the process and developing a detailed map of each stage of the manufacturing process. The inputs and desired outputs of each stage are also recorded. This format identifies inputs as either Noise or Control factors, which is critical to a Robust Engineering approach. Critical inputs to the proper output conditions can be tagged. The critical factors from the PMAP are listed on the Parameter Diagram which is shown in Figure 1.

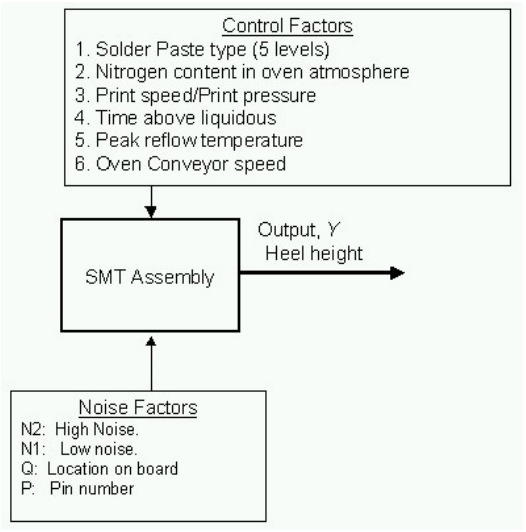

Figure 1 - Parameter Diagram Showing Critical Control and Noise Factors

The FMEA tabulates potential failure mechanisms at each stage of the process, and the causes of those failures. The level of severity of these failures to producing the proper output steps allows for the ranking of importance of process inputs. Key portions of the FMEA are shown in Figure 2.

POTENTIAL
FAILURE MODE AND EFFECTS ANALYSIS

FMEA Pro 3.2

Description Saturn Keyfob — Prepared By F. Kuhlman
Core Team M. Pepples, C. Jensen, J. Baar

Process Function / Requirements	Potential Failure Mode	Potential Effect(s) of Failure	SEV	Potential Cause(s) / Mechanism(s) of Failure	OCC	Current Process Controls	DET	RPN	Recommended Action (s)	Responsibility & Target Completion Date		Action Results: Actions Taken	New SEV	New OCC	New DET	New RPN
Function	Failure Mode	Effect	SEV	Cause	OCC	Controls	DET	RPN	Action	Resp	Comp Date	Actions Taken	New SEV	New OCC	New DET	New RPN
Proper paste volume	Paste volume too low	Intermittent, or no, electrical connection	5	Paste composition (flux chemistry)	5	None	5	125	Optimize via DOE	Jensen	2/1/02	DOE (eliminated one paste that has poor printability)	5	1	5	25
Low ionic residue	ionic residue - too much	Short or intermittent short	5	Flux chemistry - ionics too high	5	None	5	125	Optimize via DOE	Jensen	2/1/02	DOE (eliminated pastes that failed SIR test)	4	1	2	∞
Low ionic residue	ionic residue - too much	Short or intermittent short	5	Flux chemistry - insufficient rosin to bind-up free ions	5	None	5	125	Optimize via DOE	Jensen	2/1/02	DOE (eliminated pastes that failed SIR test)	4	1	2	∞
Proper wetting angles and heights	Solder joint wetting - none, open circuit	Intermittent, or no, electrical connection	5	Flux boiled off too early (ramp or soak too long)	5	None	5	125	Optimize via DOE	Pepples	2/1/02	DOE - process is fairly insensitive to oven settings (within boundary)	5	1	5	25
Proper wetting angles and heights	Solder joint wetting - none, open circuit	Intermittent, or no, electrical connection	5	Insufficient peak temp	5	None	5	125	Optimize via DOE	Pepples	2/1/02	DOE - process is fairly insensitive to oven settings (within boundary)	5	1	5	25

Figure 2 - Key portions of the Lead-free SMT Process FMEA

From the PMAP and FMEA, the following SMT process inputs were selected for testing for their effects on lead free solder joints. See Table 1.

Table 1 - Lead Free Process Inputs for Evaluation

Pb Free Process Control Factors
Paste Brand
Paste Print Speed
Oven Peak Temperature
Time Above Liquidous
Oven Conveyor Speed
Oven Nitrogen Level

The next main task in the Robust Engineering approach is the selection of noise factors. Noise factors are defined as factors that affect the output of the process but either can't be controlled, or are too expensive to control. Since wetting grade was used as the measure for process capability, key noise factors that effect wetting were selected. In the Robust approach, test cells are built at each of two noise levels, low and high. All factors that contribute favorably to the output are considered low noise, while detrimental inputs are considered high noise. Several noise factors were identified via the PMAP. Those that were suspected to have a large effect on the output of wetting and that can often be seen in production settings were selected. Table 2 shows the factors that were selected, as well as the manner by which these noise factors were implemented during the experimental runs.

Table 2 - Lead Free Process Noise Factors

Noise Factor	Low Noise	High Noise
Thickness of Paste Brick	thick stencil	thin stencil
IC Plating Metalization	Sn Plating on Cu	Ni/Pd/Au Plating on Cu
Paste Dry Out Time	reflow immediately	reflow after 1/2 hour under fan
Pin to Pin Location	multiple pins tested	multiple pins tested
Component Location on Board	multiple board locations of same part tested	multiple board locations of same part tested

A key strategy of the Robust approach is to find a combination of control factors which result in the response factor being insensitive to noise factors. For this lead free process optimization, this strategy is intended to reduce variation in wetting results over time. To study the effect of control factors, a special orthogonal array, known as an L18, was used. The L18 has the special property of evenly spreading interaction affects across all control factors. This minimizes the risk of confounding interactions while also minimizing the number of combinations to test.

For each of the 18 combinations, boards are assembled at each noise condition. The response variable is measured for each noise condition and each run. Using these results, the Signal to Noise (S/N) ratio is calculated for each of the 18 runs. The equation for the Nominal the Best S/N ratio is: $10 * Log(\bar{y}^2 / \sigma^2)$, where $\bar{y}$ is the average of the responses for that run and σ is the standard deviation of the responses for that run.

A higher S/N ratio indicates that the combination has more consistent results across noise conditions. S/N is therefore an index of 'robustness'. Dr. Genichi Taguchi defines robustness as "the state where the technology, product, or process performance is minimally sensitive to factors causing variability (either in the manufacturing or user's environment) at the lowest unit cost."[6]

The next step is to use the results of this experiment to predict the optimum combination, which is likely to be something different from one of the 18 original runs. The signal to noise is also predicted for this combination and a baseline combination. The difference between the baseline S/N and optimum S/N is the S/N Gain.

The final step is confirmation of the signal to noise for the baseline, optimum and gain. The confirmation consists of building the baseline and optimum combinations, with the same noise factors. These new boards are measured; S/N is calculated and compared to the predicted S/N and predicted Gain.

The purpose of the confirmation run is to ensure that there are no significant detrimental interactions, unknown noise factors or experimental error present. Confirmation provides confidence that the optimum combination is indeed more robust than the baseline combination.

Visual Scoring

The capability of the lead free process was based on the grade of the solder joints that the process could consistently make. A good solder joint is one that connects the component to the circuit board and properly conducts current, shows sufficient mechanical strength, and is reliable over the life of the unit. The assumption was made that a solder joint that showed good wetting and soldering characteristics was a capable lead free solder joint. The criteria for the grade of wetting were based on the industry standard IPC workmanship standards for SMT solder joints.[7] This system classifies joints

based on visually observed wetting heights and widths of the solder on the component leads. In general, better wetting is shown by greater heights or lengths. Using this same concept of 'higher the better', a visual scoring system was developed for grading the level of goodness of the lead free solder joints that were made. This scoring system for the gull wing leaded parts is shown in Figure 3.

The test vehicle selected was a 0.031 in. thick circuit board with FR4 laminate. The metallization of the board was nickel/gold (Ni/Au). The components studied included: an 8 pin SOIC (50 mil pitch) and a 0805 resistor and an 0805 capacitor. These components were placed 5 times throughout the board, in each corner and once in the middle of the board.

For each combination in the L18 experiment, four arrays were built. For each array, 3 gull wing joints, 1 resistor and 1 capacitor joints were scored.

Pull Test

Another measure of the degree of wetting of solder joints was the force required to break the joint. Pull Testing was performed on the gull-wing solder joints. While the strength of a solder joint is greatly dependent on the alloy used, pull strength differences in the same component set could result if wetting mechanisms and/or resulting inter-metallics are different due to the various flux types, printing, or reflow parameters.[8] The strength of a joint can also be considered an early life measure of the reliability of a joint. Since each DOE cell used the same alloy (within the tolerances of composition that the paste suppliers could supply), a larger force needed to break the joint was interpreted to mean a better solder joint.

For this experiment, the body package of the gull wing leaded component was cut away from the leads, resulting in a protruding lead from the circuit board. The top of the lead was clamped and pulled away from joint in the direction normal to the board. Once clamped, the joint was pulled at a rate of 0.8 mm/s until failure. The maximum force required to break the joint was recorded. Figure 4 shows an example of this process.

Score	Side Overhang max	Toe Overhang	Toe Fillet height	Side Fillet	Heel Fillet height, min	Shin Height (top of foot)	Open space (between joints)
0 = Perfect	Lead does not overhang side of land,	Toe does not overhang outer end of land	<= 100% of toe is wetted with proper angle	100% of side is wetted with proper angle	extends above lead thickness, does not fill upper lead bend, >200% of lead thickness	covers foot plus some of lead height	100% open
1 = Good	< 50 % of lead / land width	overhangs a bit, but easily meets min. electrical clearance	<75% of toe and good angle	<75% of side and good angle	>150% of lead thickness	some wetting on foot	<90% open
2 = Fair	50% of lesser of lead / land width	barely meets minimum electrical clearance	<50% of toe, and fair angle	<50% of side, and fair angle	>100% of lead thickness	no wetting on foot	<75% open
3 = NG marginal	slightly >50% of lead / land width	50-99% of minimum electical clearance	<50% of toe, bad angle	<50% of side, bad angle	< 100% of lead thickness	(not a rejectable criteria)	<50% open
4 = Bad	~75% of lead / land width	<25% of minimum electrical clearance	minimal height, some wetting	minimal height, some wetting	<50% of lead thickness		<25% open
5 = Horrible	100% off land	shorted to adjacent runner / component	zero height, no wetting	zero height, no wetting (pillow joint)	<25% of lead thickness or fills upper bend		0 % open (shorted)

Figure 3 - Visual Scoring Criteria for Gull Wing Joints

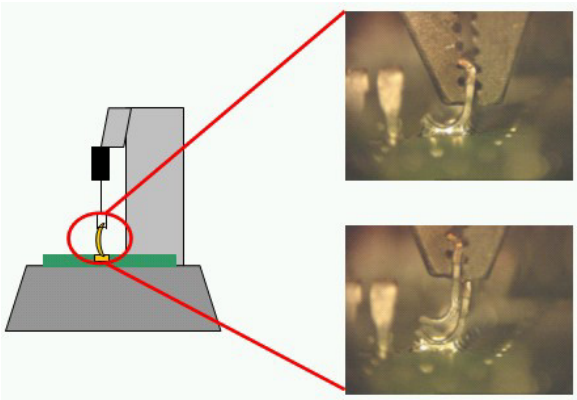

Figure 4 - Pull Test Process

Results and Discussion

Visual Scoring Results

After calculating the S/N ratio for each run of the L18 experimental design, a response table could be assembled for the visual scoring system. In this response table, the average S/N ratio for each factor at each level can be determined. This response table for S/N visual scoring for all joints is shown in Table 3. This same data is presented graphically in Figure 5.

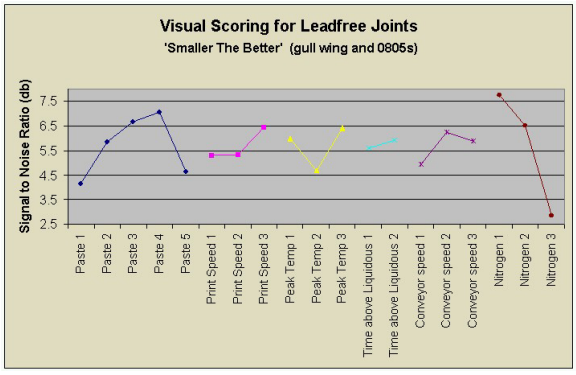

Figure 5 - Response Graph for Visual Scoring of Wetting of Lead-free joints

Figure 6 shows cross section photos of the best and worst runs of the L18 in terms of S/N ratio. These photos demonstrate how high S/N ratio corresponds to reduced variability. For run 10, the wetting heights of the joints at each noise level remain relatively consistent. Conversely, the wetting heights at the high noise level (which includes Pd/Ni/Au plated parts) for run 9 is significantly less than the wetting height at low noise level (which includes Sn plated parts).

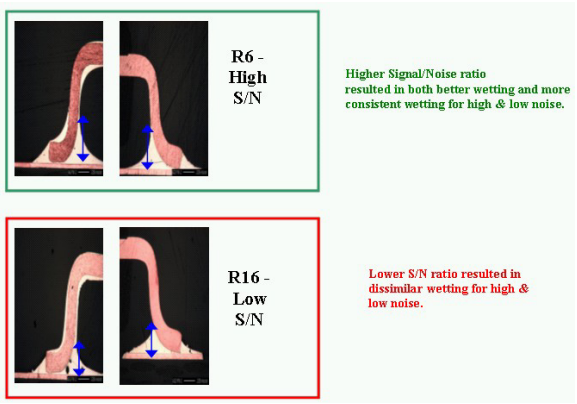

Figure 6 - Cross section photos of Best and Worst S/N of L18 runs

For each factor, the range of the S/N ratios among the different levels is shown in Table 3 as the delta. This delta value provides a measure of the relative level of influence that that particular factor has on the system output, in this case the visual score. The S/N is effected by the input factors in the following order:

N_2 Level > Paste Type > Peak Temp.> Conveyor Speed >> Print Speed> Time Above Liquidous

Since the delta values for the first four factors are significantly greater than the values for the remaining two factors, only these first four are considered significant and will be considered in the model for best settings.

Table 3 - Response Table for Visual Scoring S/N

Signal to Noise Response table - Visual Scoring						
Level	Paste Brand	Print Speed	Peak Temp	Time Above Liquidous	Conveyor Speed	Nitrogen
1	4.1	5.3	6.0	5.6	4.9	**7.7**
2	5.8	5.3	4.7	**5.9**	**6.2**	6.5
3	6.7	**6.4**	**6.4**		5.9	2.8
4	**7.0**					
5	4.6					
delta	**2.9**	**1.1**	**1.7**	**0.3**	**1.3**	**4.9**
ranking	**2**	**5**	**3**	**6**	**4**	**1**

To choose the best settings for reducing variability of the lead free soldering process with respect to noise, the setting for each factor with the largest S/N is chosen. For the solder paste type, the best S/N setting was not chosen due to the poor surface insulation resistance (SIR) performance of this paste. A paste with a better SIR value that still maintained good wetting was substituted.

The predicted S/N ratio that can be obtained from the optimal settings is calculated using the following formula:

$$S/N_{Optimal} = MaxS/N_{N2} + MaxS/N_{PasteType} + MaxS/N_{PeakTemp} + MaxS/N_{ConveyorSpeed} - 3*\overline{T}$$

where $\overline{T}$ = average all S/N in Response Table.

The predicted S/N ratio for the baseline can be obtained from the following formula:

$$S/N_{Baseline} = BaseS/N_{N2} + BaseS/N_{PasteType} + BaseS/N_{PeakTemp} + BaseS/N_{ConveyorSpeed} - 3*\overline{T}$$

where Base = Baseline Setting.

Table 4 - Optimal and Baseline Settings for Pb Free Process, and Predicted and Actual S/N for these Settings

	PASTE BRAND	PRINT SPEED	PEAK TEMP	TAL	CONV. SPEED	N_2	Predicted S/N	Actual S/N
Selected "Optimum" Settings	5	3	3	2	2	1	8.0	7.0
Baseline Settings	1	2	1	1	3	2	5.4	4.9
Gain							2.6	2.1

By comparing this optimal S/N ratio against the predicted S/N ratio for a baseline setting, it is possible to estimate the level of improvement to the lead free system that the optimal settings can provide. For this system, the baseline was chosen to be typical settings for an SMT process, especially those that allow the line to run fastest and coolest. Table 4 shows the optimal settings and baseline settings for the visual scoring output. Table 4 also shows the predicted S/N for each of these settings, along with the process gain, which is the difference between optimal and baseline S/N values.

After the "optimal" process settings were selected, a confirmation run was performed with these settings. The baseline settings were also run at this time. The gull wing IC, resistors, and capacitors were again scored and S/N ratios again calculated. The actual S/N ratios for the optimal settings and baseline settings, and the actual gain, are also shown in Table 4.

From Table 4, it can be seen that the predicted S/N values and actual S/N values are very similar for both the optimal and baseline runs. Consequently, the predicted and actual process gains are also very similar. From this it can be concluded that the optimal settings are significantly better than the baseline.

The actual process gain can be related to % process variability reduction.[10] For a given gain, the % variability reduction of the system is related by the following equation:

$$\%Variation\,\mathrm{Re}duction = (1 - \frac{1}{2}^{(\frac{GAIN}{6})}) * 100$$

For this lead free system, it is predicted that the demonstrated gain of 2.1 dB corresponds to approximately a 22 % reduction in the variation of the wetting of the solder joints, and therefore a corresponding increase in the overall quality of the lead free process.

Pull Test Results

Pull testing was performed at '0 hours' on the individual gull wing IC leads for each of the runs of the L18. The same S/N analysis as was done with the visual scoring was performed for the pull test results. However, these results did not confirm. Not confirming can be due to: 1) strong interactions between control factors, 2) strong noise factors that were not studied and not controlled, 3) pure experimental error. Because of this lack of confirmation, this metric was not used to choose the optimum process settings.

While the pull test data could not be used to discern differences between the different process settings, it was able to show significant differences between the platting types and therefore lead free metal systems used for ICs. The following three metal systems were compared:

Tin/Lead Plating with Tin Lead Solder Alloy
Tin Plating with SAC Solder Alloy
Pd/Ni/Au Plating with SAC Solder Alloy

Figure 7 shows the maximum force required to break the gull wing joints for each of these systems.

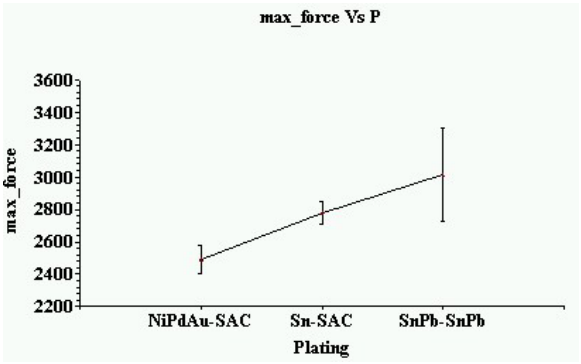

Figure 7 - Maximum Pull Strength for Leads with 3 Different Plating-Alloy Systems

This data shows that the Pd/Ni/Au plating creates a weaker joint (with respect to normal stresses) than the Sn plating when using the SAC lead free alloy. The Sn plating with the SAC alloy creates a joint that is very similar in strength to a Sn/Pb plated part soldered with Sn/Pb alloy.

Next Steps

There are several steps planned for future work in this technology.

1) Conduct a robust optimization experiment like this one on a more complicated product. This will be done to extend the learning across a larger population of component types.
2) Evaluate reliability of the leadfree joints using the optimum and baseline combinations and compare the results to tin-lead results and to customer requirements.
3) Convert a current production part to the leadfree process and gain high volume production experience and field experience.

Conclusions

Nitrogen content in the reflow oven is the most significant factor when creating high quality lead free joints. It is necessary to use highly inerted (low ppm oxygen) ovens to obtain lead free solder joints that show the least variation when considering usual processing noise. The second most significant factor to create a robust lead free manufacturing process is solder paste type. While there are a few different options, it is necessary to consider the tradeoff between those pastes that provide excellent wetting and those that have clean residues that are not a mitigating factor for electrochemical migration or dendritic growth. This is additionally true when considering lead free joints since lead free alloys tend not to wet as well as Sn/Pb alloys. This work demonstrates that there are solder pastes available that can provide both the needed wetting and the desirable level of residue cleanliness. Part plating metalization is a critical soldering process noise factor to consider when dealing with lead free. These results show Sn plated IC leads to create solder joints of equal strength to traditional Sn/Pb leads, while Ni/Pd/Au plating produced joints of lesser strength. Contributing to this reduction in joint strength is the reduced wetting that can be seen in the Pd/Ni/Au plated parts versus the Sn plated parts. Therefore, for a given product, it is necessary to consider the specific lead free metal substitute used and whether that plating metal provides a system that can withstand the stresses for that product. A robust, lead free SMT soldering process is feasible, and compensation for process noise, such as plating material, can be made by selecting the appropriate process parameters settings, especially for nitrogen level and paste type.

Acknowledgements

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